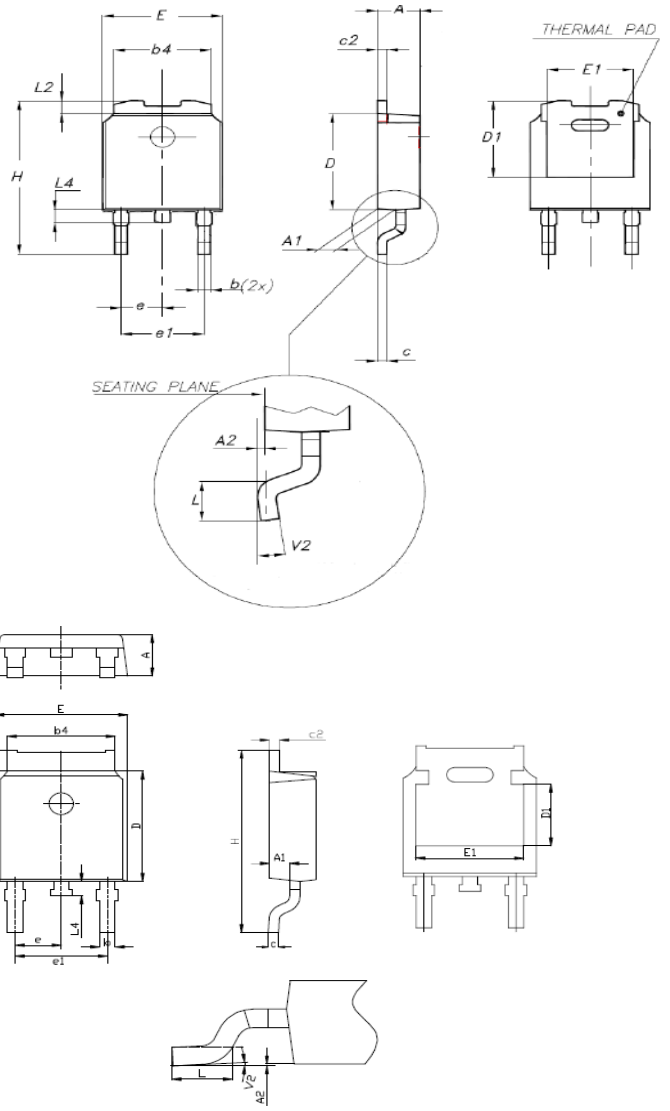
DPAK Comparison ST STD die pad vs TFME LARGE die pad

Involved Products:
GD5NB120SZ(607B), STGD5NB120SZT4

DIM.	TYPE "A" STD-ST mm			TYPE "C2" LARGE-TFME mm		
	MIN	TYP	MAX	MIN	TYP	MAX
A	2.2		2.4	2.2	2.3	2.38
A1	0.9		1.1	0.9	1.01	1.1
A2	0.03		0.23	0		0.1
b	0.64		0.9	0.72		0.85
b4	5.2		5.4	5.13	5.33	5.46
c	0.45		0.6	0.47		0.6
c2	0.48		0.6	0.47		0.6
D	6		6.2	6	6.1	6.2
D1	4.95	5.1	5.25	5.1		5.6
E	6.4		6.6	6.5	6.6	6.7
E1	4.6	4.7	4.8	5.2		5.5
e	2.16	2.28	2.4	2.186	2.286	2.386
e1	4.4		4.6			
H	9.35		10.1	9.8	10.1	10.4
L	1		1.5	1.4	1.5	1.7
(L1)	2.6	2.8	3		2.9	
L2	0.65	0.8	0.95	0.9		1.25
L3					0.51	
L4	0.6		1	0.6	0.8	1
L6					1.80	
Θ 1				5°	7°	9°
Θ 2				5°	7°	9°
R		0.2				
V2	0°		8°	0°		8°

ST

TFME



TFME = Tongfu Microelectronics

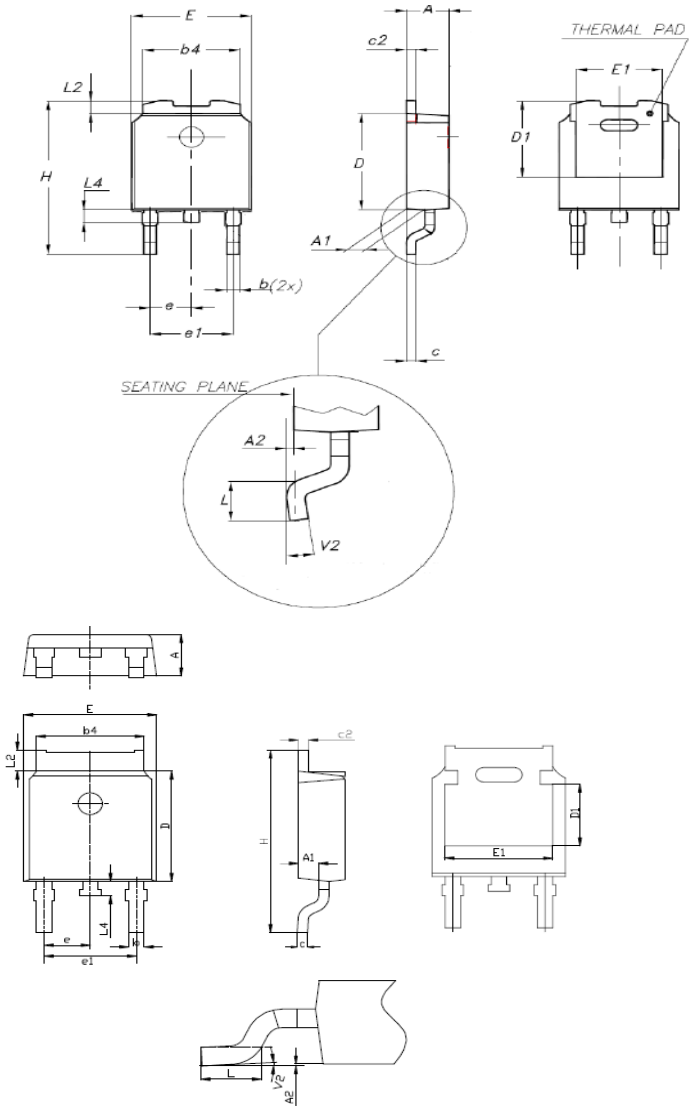
DPAK Comparison ST LARGE die pad vs TFME LARGE die pad

Involved Products:
STGD10NC60HDT4, STGD10NC60HT4, STGD14NC60KT4, STGD4M65DF2
STGD5H60DF, STGD5H60DFSF, STGD6M65DF2, STGD6NC60HDT4
STGD7NB60ST4, STGD7NC60HT4

DIM.	TYPE "A2" LARGE-ST mm			TYPE "C2" LARGE-TFME mm		
	MIN	TYP	MAX	MIN	TYP	MAX
A	2.2		2.4	2.2	2.3	2.38
A1	0.9		1.1	0.9	1.01	1.1
A2	0.03		0.23	0		0.1
b	0.64		0.9	0.72		0.85
b4	5.2		5.4	5.13	5.33	5.46
c	0.45		0.6	0.47		0.6
c2	0.48		0.6	0.47		0.6
D	6		6.2	6	6.1	6.2
D1	4.95	5.1	5.25	5.1		5.6
E	6.4		6.6	6.5	6.6	6.7
E1	5.1	5.2	5.3	5.2		5.5
e	2.16	2.28	2.4	2.186	2.286	2.386
e1	4.4		4.6			
H	9.35		10.1	9.8	10.1	10.4
L	1		1.5	1.4	1.5	1.7
(L1)	2.6	2.8	3		2.9	
L2	0.65	0.8	0.95	0.9		1.25
L3					0.51	
L4	0.6		1	0.6	0.8	1
L6					1.80	
Θ 1				5°	7°	9°
Θ 2				5°	7°	9°
R		0.2				
V2	0°		8°	0°		8°

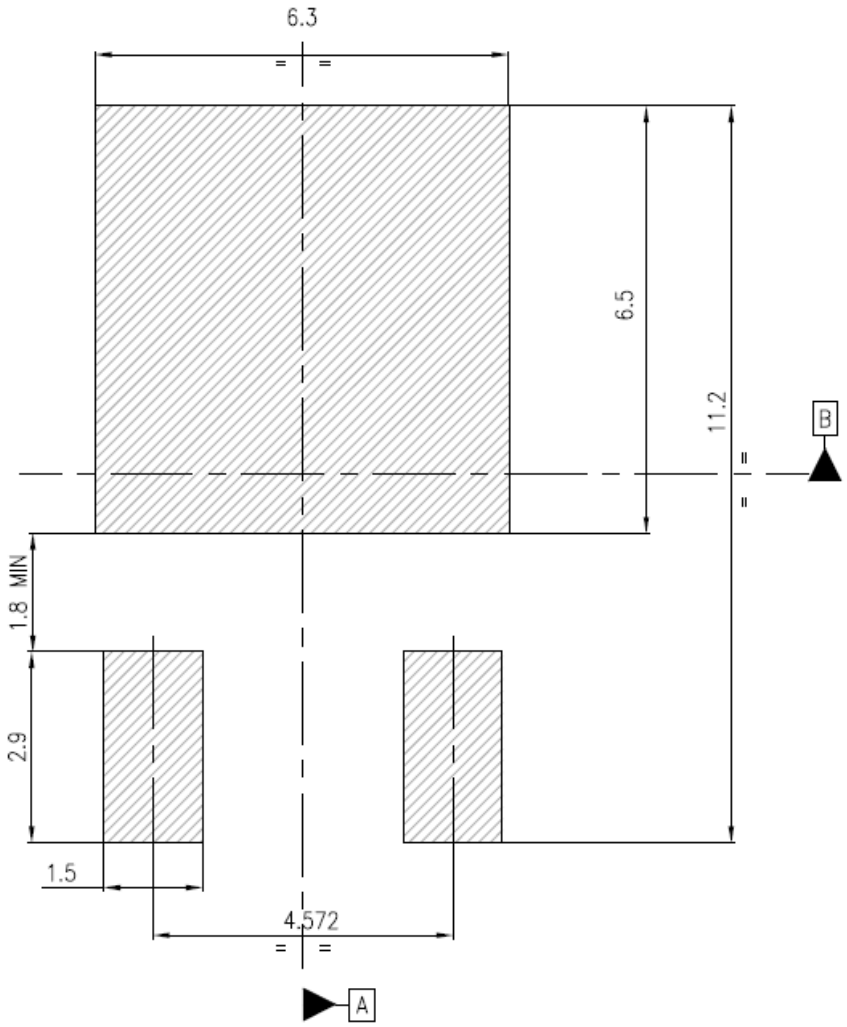
ST

TFME



TFME = Tongfu Microelectronics

DPAK Unchanged Recommended Footprint



Dear Customer,

Continuing in the aim of a constant process improvement, please be informed that we're going to use DPAK Automatic Assembly/Testing for Selected IGBTs in Tongfu Microelectronics (China). DPAK products, manufactured in Tongfu Microelectronics (China), guarantee the same quality and electrical characteristics as reported in the relevant data sheets. Devices used for qualification are available as samples.

The involved product series and affected packages are listed in the attached file.

Any other Product related to the above series, manufactured in Tongfu Microelectronics (China), even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report plan is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 48-2017.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family Description	Package	Part Number - Test Vehicle
IGBT	DPAK	STGD5H60DFSF STGD6NC60HDT4 STGD7NC60HT4

Change implementation schedule:

The production start and first shipments will be implemented according to our work in progress and materials availability:

Product Family	1st Shipments
IGBT	From Week 10-2018 *

* Due to the current long delivery time, we need to speed-up PCN approval.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 days period will constitute acceptance of the change (Jedec Standard No. 46-C). In any case, first shipment may start earlier with customer written agreement.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of IGBTs manufactured in Tongfu Microelectronics (China) subcontractor will be ensured by "GF" as first digits of the trace code, internal code (Finished Good) and Q.A. number.

Sincerely Yours.

Reliability Report Plan

DPAK IGBT and IGBT+Diode Assembly Capacity Expansion
in Tongfu Microelectronics (China)
INDUSTRIAL

General Information	
Product Lines:	IGBT EI6201 - Diode F62B IGBT IV6201 - Diode F62I IGBT IV6401
P/N:	STGD5H60DFSF STGD6NC60HDT4 STGD7NC60HT4
Product Group:	ADG
Product division:	Power Transistor Division
Package:	DPAK
Silicon Process techn.:	IGBT Planar IGBT Trench

Locations	
Wafer Fab and EWS Plant:	*IGBT: Catania (Italy)* *Diode:Tours (France)*
Assembly and testing plant:	*Tongfu Microelectronics (China)*
Reliability Lab:	*ADG - Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	November 2017	8	A. Settinieri	C. Cappello	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify DPAK IGBT and IGBT+Diode assembled in TONGFU Microelectronics (China)

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

IGBT Planar / IGBT Trench

4.2 Construction note

D.U.T.: STGD5H60DFSF PACKAGE: DPAK

Wafer/Die Information	
Technology	IGBT Trench - Diode
Wafer Fab	IGBT Catania (Italy) - Diode *Tours (France)*
Die finishing back side	IGBT Al/Ti/NiV/Ag
Die size	IGBT: 2510 x 1950 µm^2 / Diode: 1100 x 1100 µm^2
Metal	IGBT AlCu
Passivation type	GBT SiN (nitride)

Assembly/Testing information	
Assembly site	Tongfu Microelectronics (China)
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach material	Soft Solder UMICORE Pb/Sn/Ag
Wire bonding process	Ultra Thermosonic
Wires bonding materials	Gate: Al (5mils) Source: Al (15mils)
Lead finishing/bump solder material	Pure Tin

D.U.T.: STGD6NC60HDT4 PACKAGE: DPAK

Wafer/Die Information	
Technology	IGBT Planar - Diode
Wafer Fab	IGBT Catania (Italy) - Diode *Tours (France)*
Die finishing back side	IGBT Cr/Ni/Ag
Die size	IGBT 1690 x 2620 µm^2 / Diode: 1100 x 1100 µm^2
Metal	IGBT AlSi
Passivation type	IGBT SiN (nitride)

Assembly/Testing information	
Assembly site	Tongfu Microelectronics (China)
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach material	Soft Solder UMICORE Pb/Sn/Ag
Wire bonding process	Ultra Thermosonic
Wires bonding materials	Gate: Al (5mils) Source: Al (5mils)
Lead finishing/bump solder material	Pure Tin

D.U.T.: STGD7NC60HT4 **PACKAGE: DPAK**

Wafer/Die Information	
Technology	IGBT Planar
Wafer Fab	IGBT Catania (Italy)
Die finishing back side	IGBT Cr/Ni/Ag
Die size	IGBT 3500 x 2880 µm^2
Metal	IGBT AlSi
Passivation type	IGBT SiN (nitride)

Assembly/Testing information	
Assembly site	Tongfu Microelectronics (China)
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach material	Soft Solder UMICORE Pb/Sn/Ag
Wire bonding process	Ultra Thermosonic
Wires bonding materials	Gate: Al (5mils) Source: Al (10mils)
Lead finishing/bump solder material	Pure Tin

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot	Part Number	Silicon Lines	Package	Wafer Fab	Assy Plant	Comments
1	STGD5H60DFSF	EI62	DPAK	Catania (Italy)	Tongfu Microelectronics (China)	
2	STGD6NC60HDT4	IV62				
3	STGD7NC60HT4	IV64				

5.2 Reliability test plan summary

#	Stress (Abrv)	PC	Std ref.	Conditions	Sample Size (S.S.)	Steps	Failure/SS		
							Lot 1	Lot 2	Lot 3
1	**TEST**		User specification	All qualification parts tested per the requirements of the appropriate device specification.			0/190	0/190	0/190
2	**External visual**		JESD22 B-101	All devices submitted for testing			0/190	0/190	0/190
Silicon Oriented Test									
3	**HTRB**	N	JESD22 A-108	Tj = 150°C ; BIAS = 480V	45 x lot	1000H	04/2018	04/2018	04/2018
4	**HTGB**	N	JESD22 A-108	Tj=150°C ; BIAS= 25V	45 x lot	1000H	04/2018	04/2018	04/2018
Package Oriented Test									
5	**Pre-conditioning**		JESD22 A-113	Dryng 24H @ 125°C Store 168H @ TA=85°C RH=85% IR Reflow @ 260°C 3 times	All devices to be subjected to H3TRB, TC, AC	Final	04/2018	04/2018	04/2018
6	**TC**	Y	JESD22 A-104	TA=-65°C TO 150°C 1 HOURS / CYCLE	25 x lot	500cy	04/2018	04/2018	04/2018
7	**AC**	Y	JESD22 A-102	TA=121°C ; PA=2ATM	25 x lot	96H	04/2018	04/2018	04/2018

8	**H3TRB**	Y	JESD22 A-101	TA=85°C ; RH=85% BIAS=80V	25 x lot	1000H	04/2018	04/2018	04/2018
9	**IOL**	N	MIL-STD-750 Method 1037	ΔTj ≥105°C	25 x lot	10Kcy	04/2018	04/2018	04/2018
10	**ESD**		ESDA-JEDEC_ JES-001 ANSI-ESD S5.3.1	CDM / HBM	3 x lot		04/2018	04/2018	04/2018
11	**Physical Dimension**		JESD22 B-100		30 x lot		0/30	0/30	0/30
12	**Solderability**		J-STD-002		10 x lot		0/10	0/10	0/10
13	**Terminal Strength**		MIL-STD-750 Method 2036		30		0/30	0/30	0/30
14	**Bond Shear**		JESD22 B-116		10 bonds from min of 5 devices		0/5	0/5	0/5
15	**Resistance to Solder Heat**		JESD22 A-111		12		0/12	0/12	0/12

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias **HTGB / HTFB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
IOL / TF Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB/THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.